



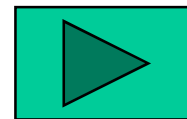
R和统计在半导体界的应用

中芯国际 — 良率管理系统

2009-12-12

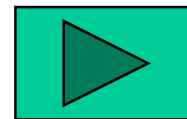
Applied R and Statistics for Semiconductor

➤ Semiconductor introduction

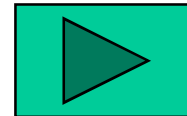


➤ R/Statistics applications

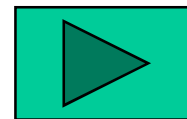
➤ Some recent cases



➤ Patent: Product Bit Analysis



➤ Patent: WAT Classification Analysis



Thank you 谢谢

Q&A 请您提问 

基本资料

林光启

学历:

美国Texas A&M University 统计硕士,
University of Southern California MBA

工作经验:

Stata Corp, 客服工程师

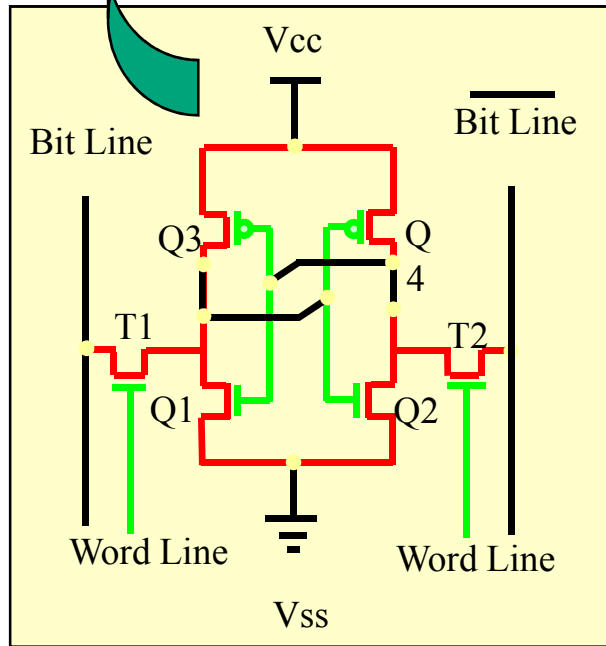
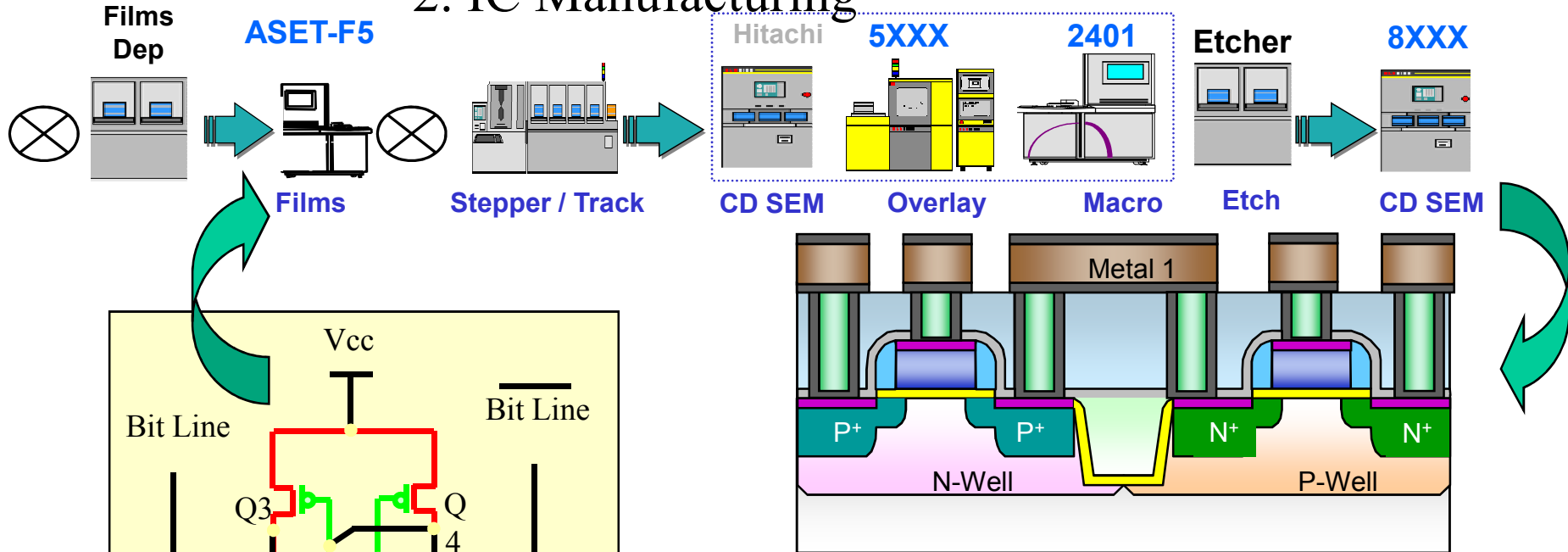
PDF Solutions, 研发工程师

中芯国际, 良率管理部门主管

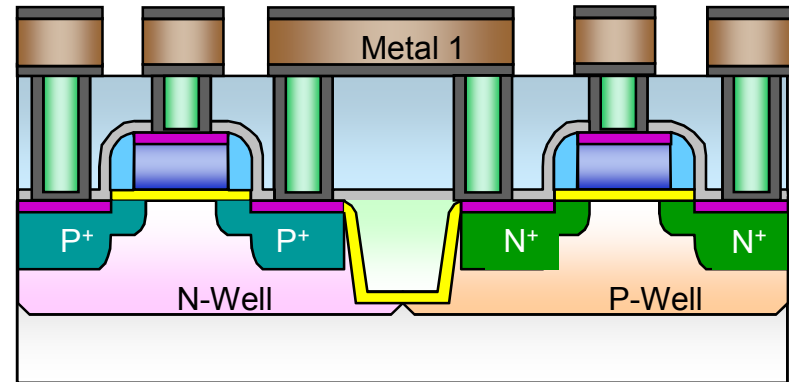


Integrated Circuit (IC) Manufacturing

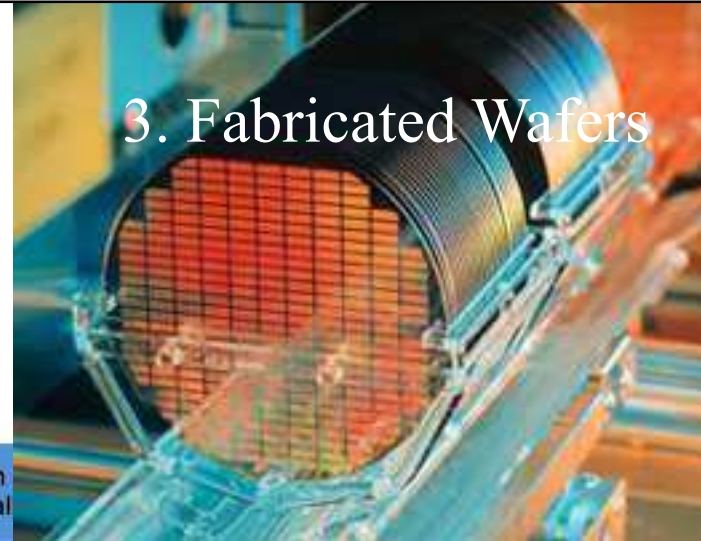
2. IC Manufacturing



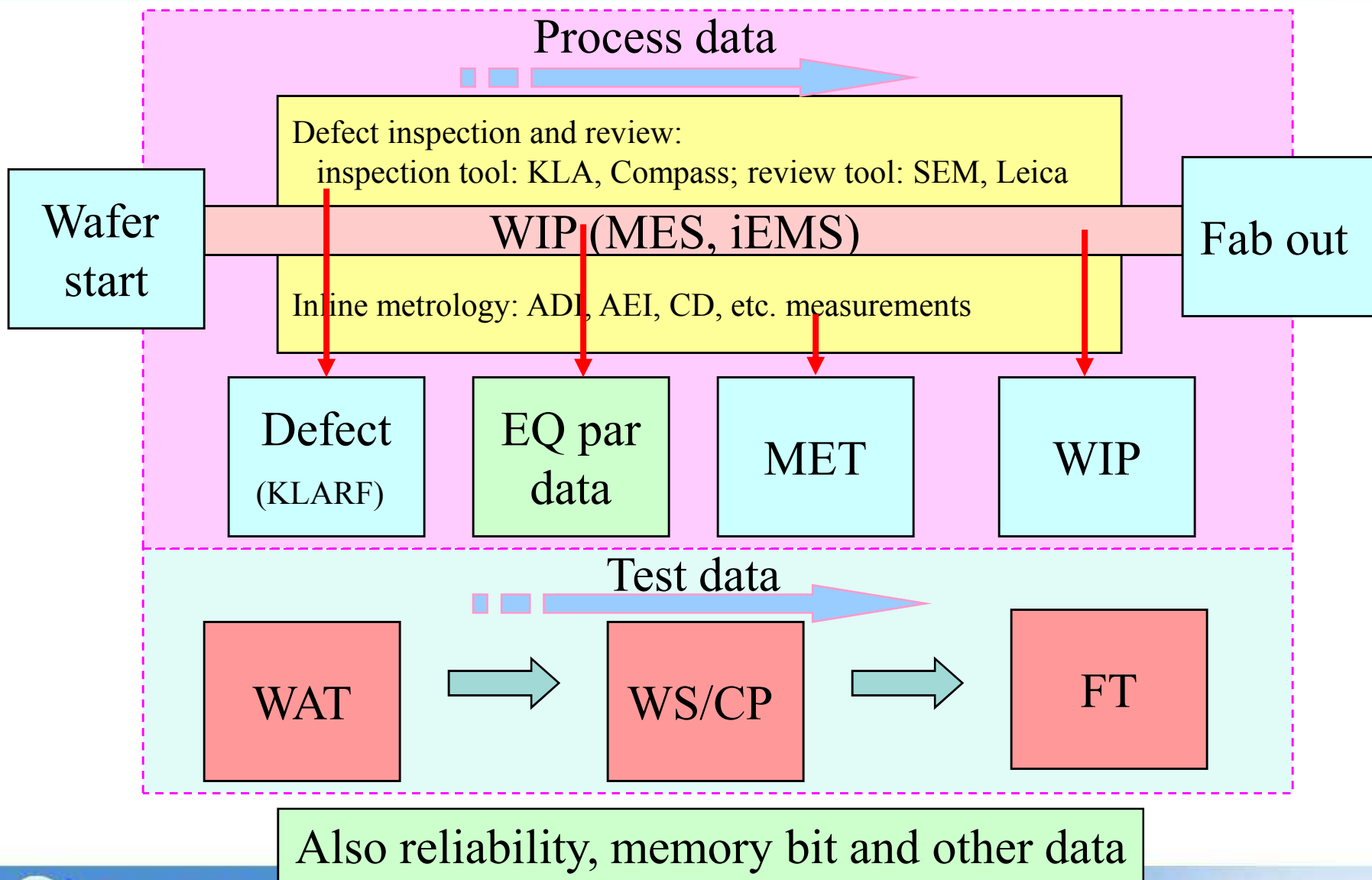
1. IC Design



3. Fabricated Wafers



Semiconductor Manufacturing Data Flow



Complications...

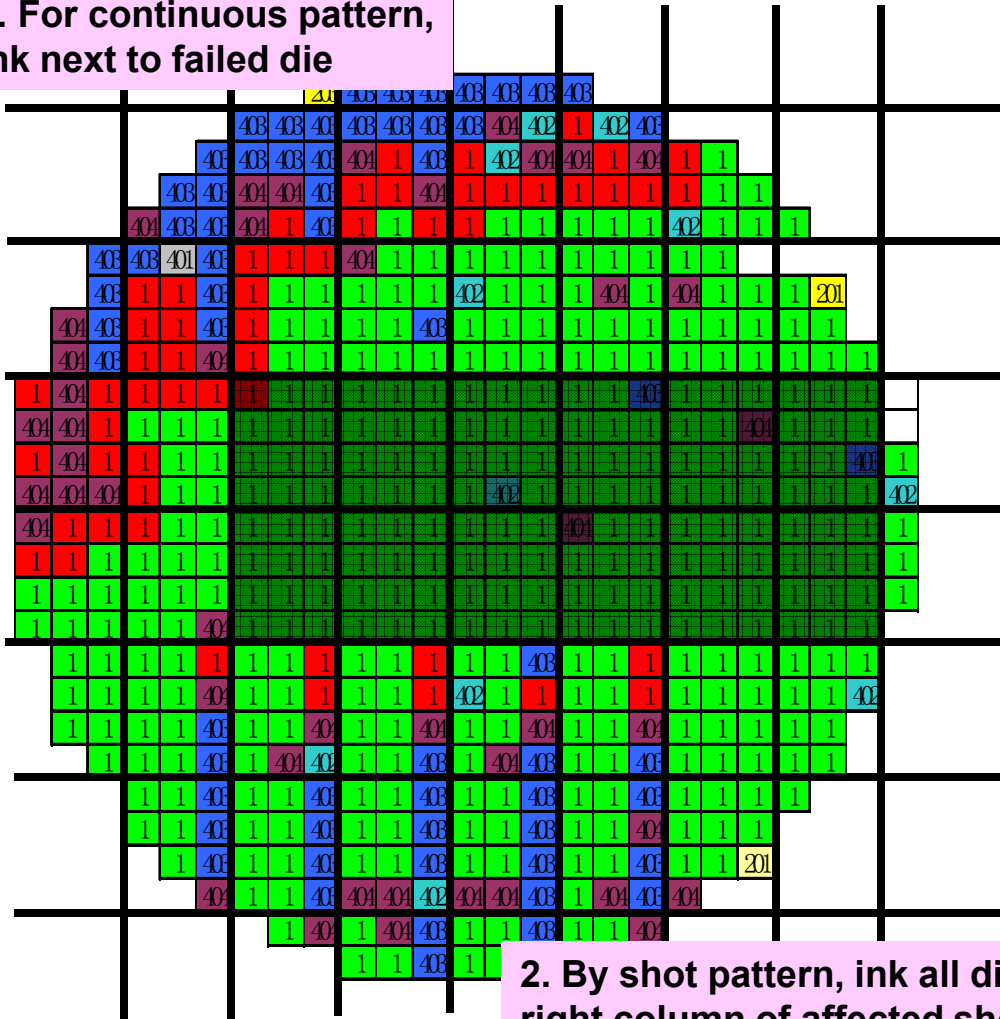


- Huge and complex production data
 - Mass product weekly volume:
 - CP: 50 lots * 25 wafers * 500 dies = **625K dies**
 - WAT: 50 * 25 * 80 parameters * 5 sites = **500K measurements**
 - WIP: **400+ steps, continuous equipment parameter data**
 - Complexity
 - **Data complexity**
 - Yield bins and zones, WAT scale, defect within-die location
 - **Relational complexity**
 - CP-WAT link at wafer/site levels, CP/bit-Defect, CP-WIP
- Extreme valuable information
 - Large stake: 150K+ wafers / month
 - Efficiency: generate reports from hours/days to automated report
 - **Free engineers to do engineering!**

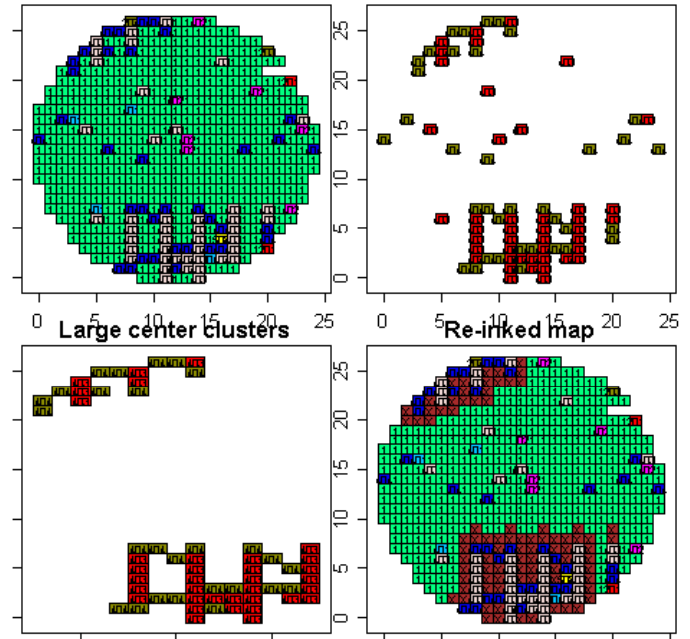
Solve 4 days earlier with 50 wafers/day = 200 wafers!

Wafermap Application – Re-ink At-Risk Die

1. For continuous pattern, ink next to failed die



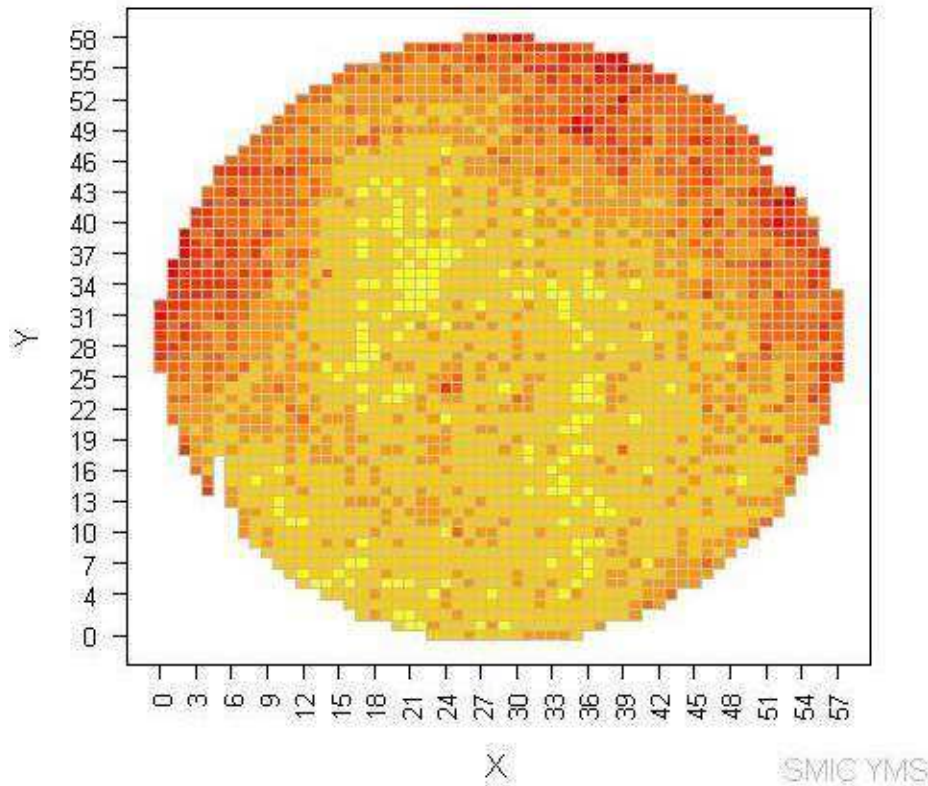
2. By shot pattern, ink all die in right column of affected shot.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
1																									
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Wafermap Application – View Parameter Pattern

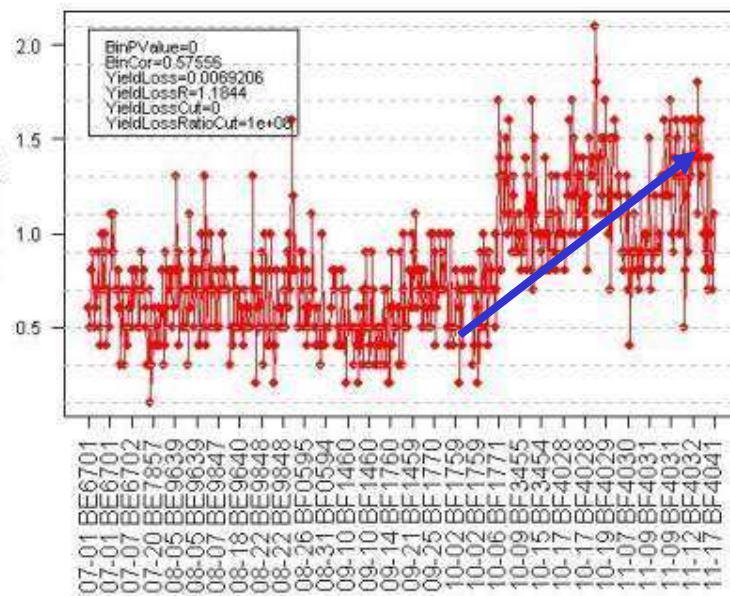


Item	Low	Up	Color
2000	0	0.0002	8
2000	0.0002	0.0005	7
2000	0.0005	0.0008	6
2000	0.0008	0.0011	5
2000	0.0011	0.0014	4
2000	0.0014	0.0017	3
2000	0.0017	0.002	2
2000	0.002	0.005	1
2000	0.005	10	black
2001	0	0.0002	9
2001	0.0002	0.0005	8
2001	0.0005	0.0008	7
2001	0.0008	0.0011	6
2001	0.0011	0.0014	5
2001	0.0014	0.0017	4
2001	0.0017	0.002	3
2001	0.002	0.005	2
2001	0.005	10	1
2002	-10	-0.002	black

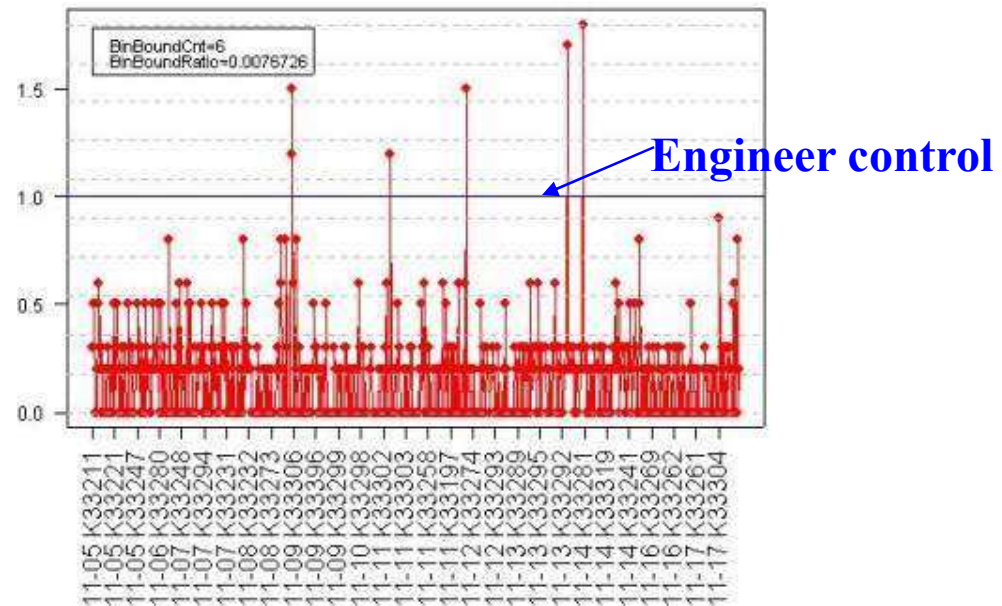


Trend Chart Application – Monitor Yield Bins

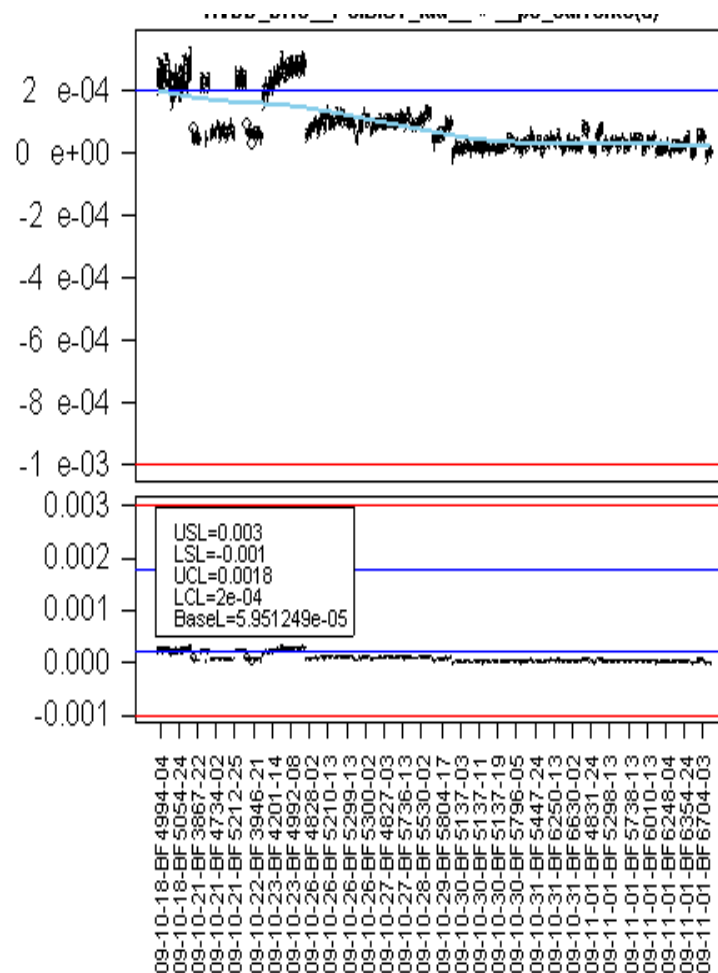
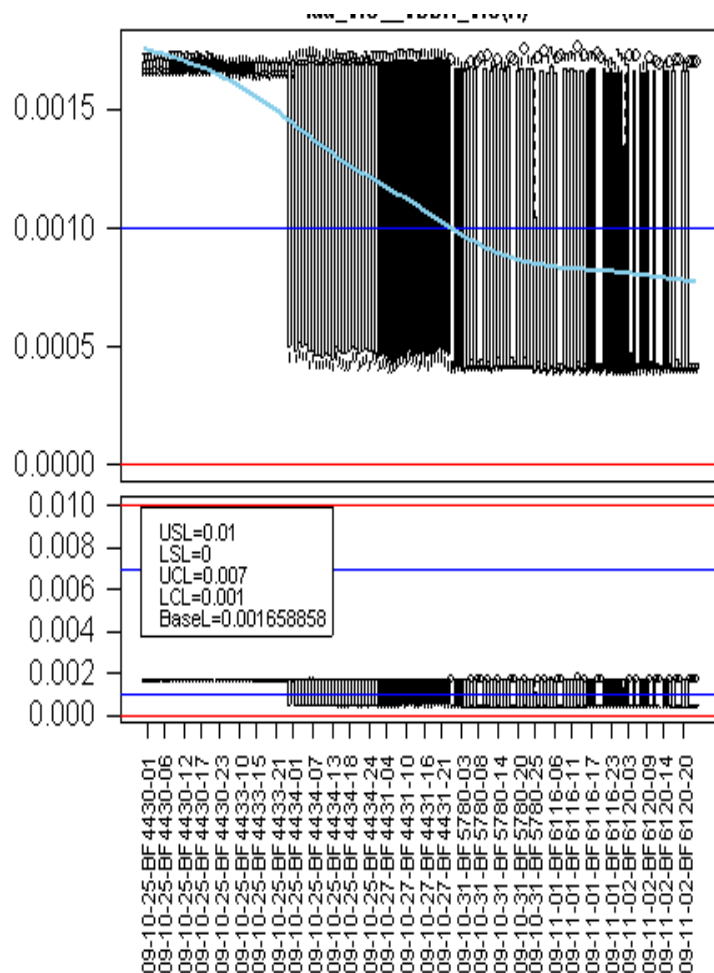
- Trend up



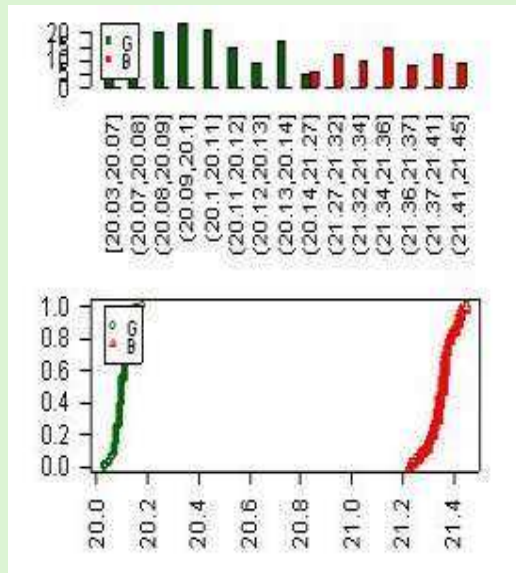
- Out of bound



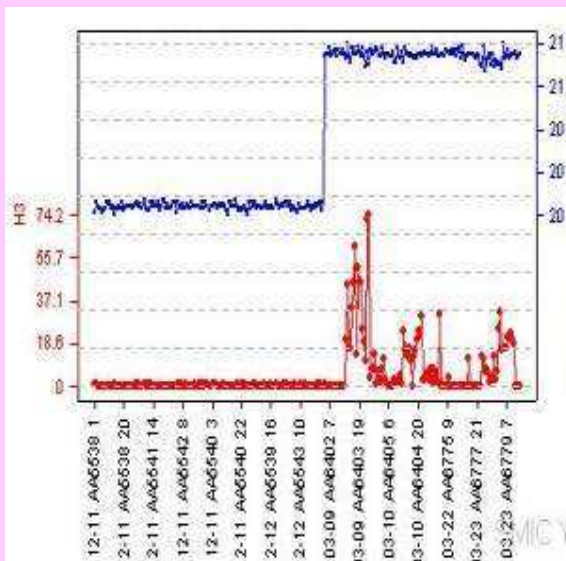
Trend Chart Application – Monitor E-Test Data



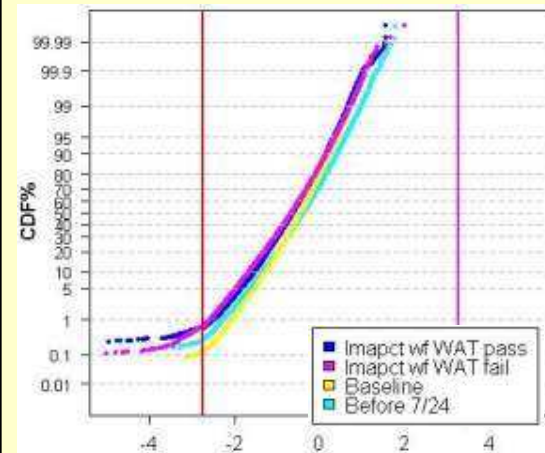
Comparison Applications



Good/Bad comparison



Parameter trends comparison

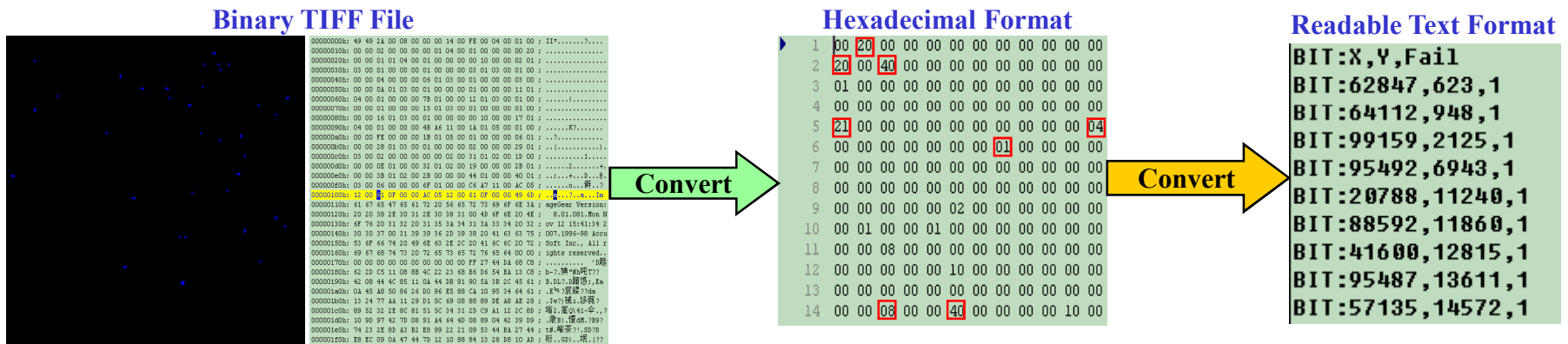


Experiment comparison

- Identify statistically and engineering significant signals out of hundreds, thousands, and more parameters

Memory Bit Data

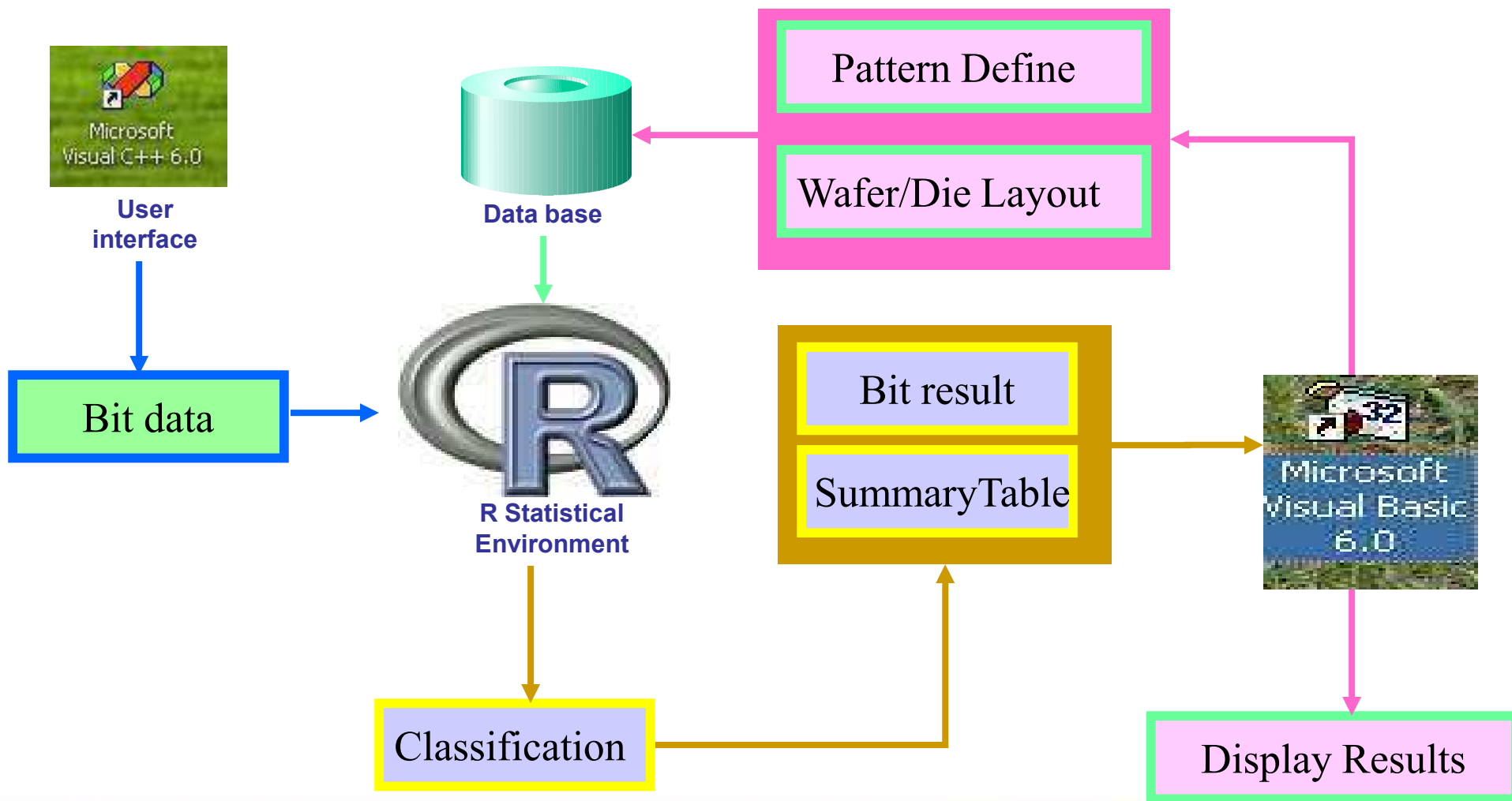
- Memory bit data characteristics
 - Lattice-like 0/1 (pass/fail) data
 - Different coordinate systems: electrical address, logic address, physic address



- Universal demands of **Product Bit Analysis(PBA)**
- All Memory/Flash and Logical SRAM products need **Bit Analysis** to find out EFA (electrical failure analysis) root cause



Patent: Product Bit Analysis System



PBA – Defining Bit Fail Pattern

Pattern Define

Areas Define

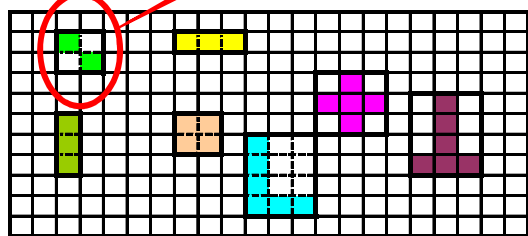
Cross Define

Line Define

Point Define

Pattern Edit

Major point fail patterns



Point Pattern Define

Pattern Select
Product_ID: SP130-01
Pattern Name: Ajust
Type Select: Point
Pattern check by: Block
Filter Select: Y

Pattern Define
Min Bit: 2
Max Bit: 2
H_offset: 1
V_offset: 1
Cont_H:
Cont_V:
H_E/O: Any
V_E/O: Any
Min Sep: 1

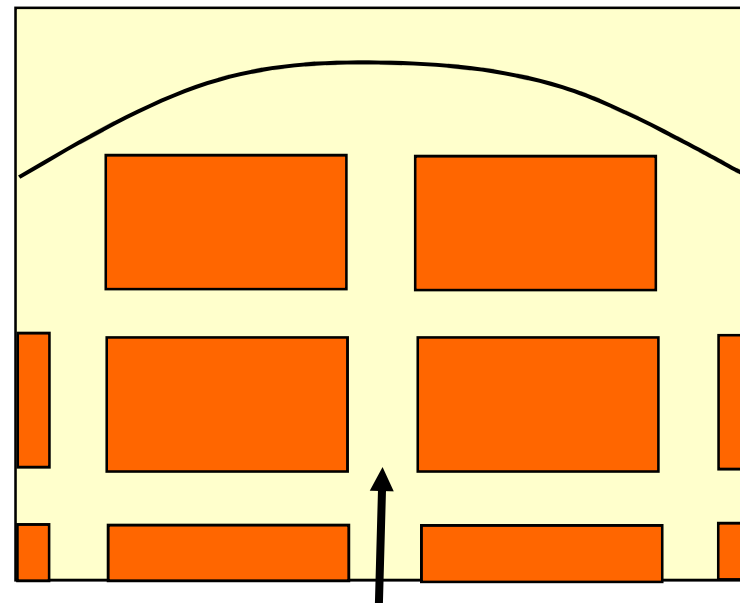
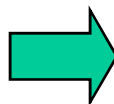
Save Close Query Table Delete Err_Rec

id	sequ	product id	name	type	check area	filter	min bits	max bits	h offset	v offset	h continuous
52	16	SP130-01	Sbit	Point	Block	Y	1	1	0	0	0
51	14	SP130-01	RTB	Point	Block	Y	2	2	0	0	1
50	15	SP130-01	CTB	Point	Block	Y	2	2	0	0	0
48	13	SP130-01	TriBit	Point	Block	Y	3	3			1
49	12	SP130-01	QBit	Point	Block	Y	4	4	1	1	1

❖ Overall fail patterns define

❖ Friendly configure UI

Wafer Acceptance Test (WAT) Data



Scribe-line

WAT:

- Electrical test data from test structures

A diagram showing two test structures. On the left is a cross-shaped structure with a purple square in the center. On the right is a structure with a central zigzag line between two grey rectangular blocks labeled "2" and "3".

Test Structures

Patent: WAT Classification Background Information

- **WAT 与 CP 在实际中的应用**

- 在晶片的制造过程中，芯片之间最终会切割掉的区域 (Scribe-line)，会放一系列的测试结构，用于记录生产过程及设备状况的信息。在整个晶片生产完成后，针对晶片上的测试结构会进行一系列的电性测试，得到的结果即为 Wafer acceptance test (WAT) 数据。
- 通常 WAT 数据具有代表晶片好坏的特性，针对 WAT 数据和 CP 数据的统计方法在 Dynast 系统中已得到广泛的应用。

- **提出问题的背景**

- 基于良率 (CP) 数据与 WAT 数据通常有很强的相关性，工程师在测完WAT时就可以对晶片的良率有些概念。但因为问题的复杂性，工程师通常只有些模糊的概念。

- **本专利解决的问题**

- 本专利运用统计和数据库挖掘的手法从历史CP和WAT数据得到它们综合的相关性，然后从新晶片的WAT结果来对它们未知的CP结果做个好或坏的预测。

Patent: WAT Classification Background Information

- 基于 WAT 数据分析的已有方法

- WAT的测试结果反映了整个生产过程的总体状况， WAT参数取值与产品良率有很强的相关性，对WAT参数进行统计分析能使我们得到关于产品良率的诸多信息。
- WAT参数众多（上百到数百个）而且参数之间有较强的交互效应，它们的统计性质也变的相对复杂。
- 现有的针对WAT参数的统计工具主要有比较分析、相关性分析，比如对不同条件下生产的晶片的WAT参数作比较分析，看不同条件下的WAT参数是否有明显差异；将WAT参数与CP数据、WS数据、iEMS数据等做相关性分析，可以找出有相关性的因素。
- 已有分析方法均是基于现有历史数据对产品的生产及设备状况特征进行分析。

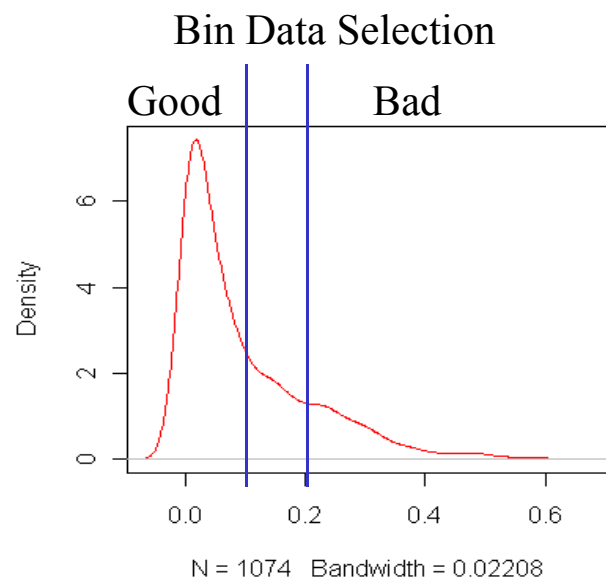
- 已有方法的不足之处

- 利用历史数据对产品特征进行预测，现有的统计工具还不能实现。
- 本专利正是基于预测分类问题而提出的解决办法 。

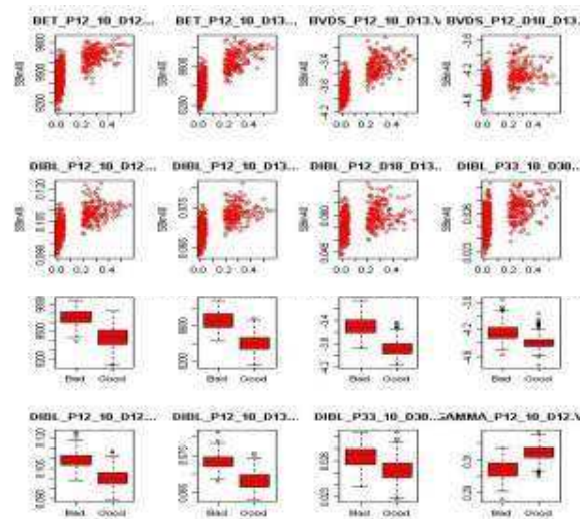
WAT Classification Analysis

- Problem
 - Predict good/bad yield group from WAT data
- Model building
 - Based on historical data and good/bad wafer groups
 - Select “useful” WAT parameters, 筛选WAT参数
 - Principle Component Analysis, 主成分分析
 - Discriminant analysis, 判别分析

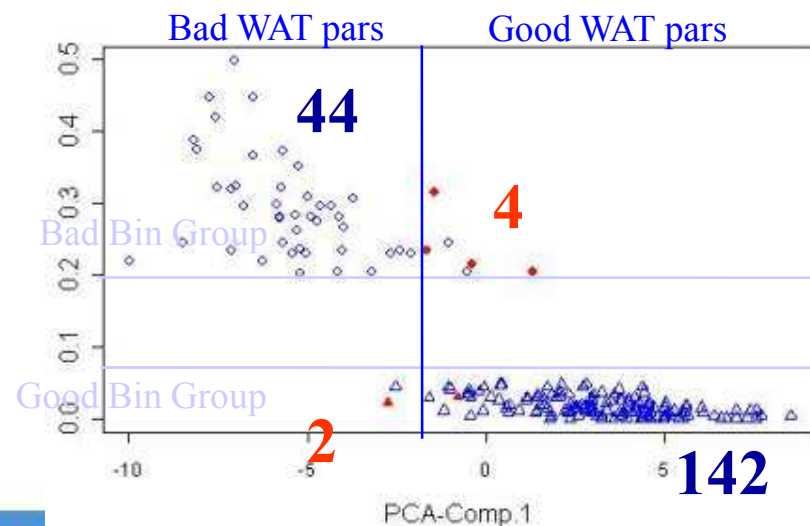
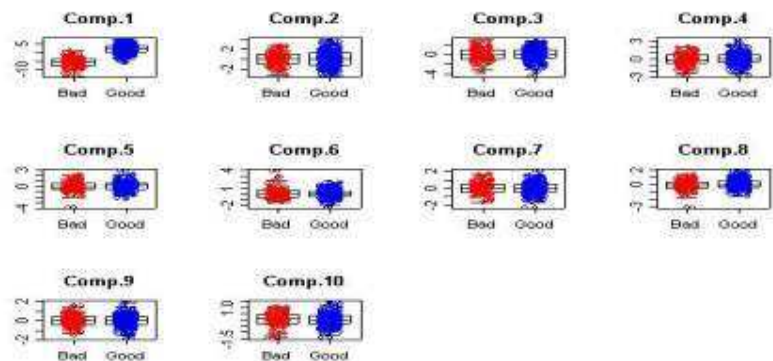
WAT Classification Example



WAT Selection



PCA



Excellent Cross-Validation Results



#0770 实验流程图形五：

模型组： **Good Wafer Count: 370; Bad Wafer Count: 136**

测试组： **Good Wafer Count: 144; Bad Wafer Count: 48**

判别分析分类结果：

	Orig. Good	Orig. Bad
Class. Good	142	4
Class. Bad	2	44

说明：以上分类结果表明，对Original Good Wafer作预测的正确率达到了98.6%，对Original Bad Wafer作预测的正确率达到了90.9%。预测发生错误的Wafer主要处于好组与坏组的相交地带。